Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A0**
2. **A1**
3. **A2**
4. **N. E1**
5. **N. E2**
6. **N. E3**
7. **N. Y7**
8. **GND**
9. **N. Y6**
10. **N. Y5**
11. **N. Y4**
12. **N. Y3**
13. **N. Y2**
14. **N. Y1**
15. **N. Y0**
16. **VCC**

**.057”**

**2 1 16 15 14**

**3**

**4**

**5**

**6**

**7**

**8 9 10**

**13**

**12**

**11**

**MASK**

**REF**

**13602F**

**.070”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential: VCC or Float**

**Mask Ref: 13602F**

**APPROVED BY: DK DIE SIZE .057” X .070” DATE: 3/9/23**

**MFG: RCA/HARRIS THICKNESS: .021” P/N: 54HCT138**

**DG 10.1.2**

#### Rev B, 7/19/02